A MONOLITHIC L-BAND LIMITING AMPLIFIER AND DUAL-MODULUS PRESCALER GaAs INTEGRATED CIRCUIT

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ABSTRACT

We present fabrication details, RF-yield results, and RF performance vs. temperature for an ECL-compatible, L-band, limiting dual-modulus (÷ 10/11) prescaler. This new process for monolithic integration of analog and digital circuit functions uses refractory self-aligned gate FET technology. When tested with -22 dBm input signal power, one lot of six wafers had a total RF chip yield of 19%, with a best-wafer yield of 43%. The average operating frequency was 1.45 GHz (SD = 51 MHz) with an average power dissipation of 696 mW (SD = 23 mW).

INTRODUCTION

Microwave and digital GaAs circuit functions are successfully implemented monolithically for the first time using a fully planar refractory self-aligned gate (SAG) field-effect transistor (FET) technology. This new process is demonstrated by fabricating an ECL-compatible, L-band limiting dual-modulus (÷ 10/11) prescaler GaAs integrated circuit. Below we present the details of the fabrication process, dc- and RF-yield results, and RF performance vs. temperature for this circuit.

FABRICATION PROCESS

The combined analog and digital process, which is a melding of the ITT analog [1] and digital [2] processes, is illustrated in Fig. 1. This fully planar process (no gate recessing is employed for FET fabrication), employs selective ion implantation into undoped LEC substrates (Fig. 1a). Four selective implants are required, one each for the microwave, D-mode digital and E-mode digital FET's, and a fourth for resistors. Titanium tungsten nitride (TiWN) is then deposited by reactive sputtering [3]. This material forms the thermally stable gate electrode, and it is patterned into 'T-gate' structures by reactive-ion etching using an Ni etch mask defined by liftoff (Fig. 1b).

After the 'T-gate' structures have been defined, the wafer is patterned with photoresist in preparation for the n+ implant (Fig. 1c). In particular, a stripe of resist overlaps the 'T-gate' on the analog FET's; whereas, the digital FET's have no resist stripe. This results in the n+ implant for the analog FET being asymmetric: self-aligned to the 'T-gate' on the source side, but separated from it on the drain side. Therefore, the separation between the gate and n+ on the source side is nominally 0.2 μm, which results in low parasitic source resistance; however, the separation between the gate and n+ on the drain side is increased to approximately 1 μm by the resist stripe, which increases the output resistance and breakdown voltage of the analog FET. Hence, an asymmetric n+ implant is used to improve the analog FET performance, while a symmetric n+ implant for both types of digital FET's results in the best digital performance.

After implant and resist removal, the wafer is capped with SiON and annealed to activate all implants (Fig. 1d). The SiON is then planarized using reflowed resist and a CF_4/O_2 plasma etch-back. This exposes the entire gate electrode for electrical contact by the overlay metal. In addition, ohmic contact metal is embedded into the planarized dielectric and alloyed (Fig. 1e).

Next Ti/Au first level metal is overlayed over the entire width of the gate electrodes (Fig. 1f). Since it has both a larger cross-sectional area and a higher electrical conductivity than the underlying TiWN Schottky contact, this overlayer dramatically reduces the gate

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resistance. Because the Au-based overlayer is insulated from the GaAs surface by the planarizing dielectric, both the alignment tolerance and linewidth constraint on the overlayer can be relaxed. In addition to reducing the FET gate resistance, this layer overlays the ohmic contact metal to reduce its sheet resistance and serves as first-level interconnect metallization for the entire IC (Fig. 1f).

A second level of TiPdAu interconnect metal is defined on a silicon nitride intermetal dielectric, which also serves as the MIM capacitor dielectric (Fig. 1g). Finally, a third level of plated Au interconnect metal is added to define microwave transmission lines and airbridges for low capacitance cross-overs (Fig. 1h). The wafers are then thinned to 125 μm; if required, backside through-vias are etched to the FET source pads using a Ni etch mask, and the backside is plated (Fig. 1h).

RESULTS AND DISCUSSION

The die used for this circuit contained three separate chips: the limiting amplifier; the dual-modulus (÷ 10/11) prescaler; and the monolithically integrated limiting amplifier/prescaler circuit. The RF performance and yield data that follow were obtained by measuring the individual performance of all three types of chips on one lot of six wafers.

Figure 2 shows a plot of the layout of the monolithically integrated amplifier/prescaler (Fig. 2a), in addition to the gain vs. frequency (Fig. 2b) of just the limiting amplifier as a separate chip. (The layout of the separate limiting amplifier chip is identical to the limiting amplifier part of the circuit shown in the integrated layout.) Figure 2b shows the gain vs. frequency of the highest-gain and lowest-gain amplifiers of the 18 limiting amplifiers which met the RF-pass criterion: RF gain within ± 1.5 dB of the average RF gain over the wafer. These 18 amplifiers are 72% (18/25) of the dc-good chips from the wafer and the dc yield was 60%. Thus the total limiting amplifier chip yield to RF spec was about 43%.

Table 1 presents the measurement parameters and the resulting RF performance and yield for the separate prescaler chips from the two wafers with the best yield. As shown in the table, the DCFL dual-modulus (÷ 10/11) prescalers were tested to 2.5 GHz and the average yield was 80%.

TABLE 1

Dual-Modulus (÷ 10/11) Prescaler Performance and Yield

PARAMETERS	WAFER # 2		WAFER #4	
	MEAN	BEST	MEAN	BEST
Drain Supply Voltage, V_{DD} (V)	5.0	5.0	5.0	5.0
Drain Supply Current, I_{DD} (mA)	26.1	28.6	25.0	24.7
Emitter Supply Voltage, V_{EE} (V)	-5.2	-5.2	-5.2	-5.2
Emitter Supply Current, I_{EE} (mA)	5.4	5.6	6.7	6.0
Termination Supply Voltage, V_{TT} (V)	-3.0	-3.0	-3.0	-3.0
Termination Supply Current, I_{TT} (mA)	38.3	36.0	36.0	33.9
Power Dissipation (mW)				
Internal	131	143	125	124
Total (incl. output drivers)	208	219	203	199
Max. Operating Frequency (GHz)	2.12	2.52	1.73	2.06
Yield	27/35 77%	---	29/35 83%	---

Figure 3 shows the maximum frequency of the monolithically integrated limiting amplifier/prescaler chip vs. input power. For inputs from -22 dBm to 10 dBm, all RF-good chips were fully functional up to 1 GHz.

Table 2 presents RF performance and yield data of the combined analog and digital chip. All measurements were made with a specified -22 dBm input signal power using the supply voltages shown in Table 1. Under these test conditions, the three wafers in Table 2 had an average maximum operating frequency of 1.45 GHz (SD = 51 MHz) with an average power dissipation of 696 mW (SD = 23 mW). Since the average RF yield of the three wafers was 37% and the wafer yield from processing was 50% (3 of 6), the total lot RF yield was 19%. This yield is unexpectedly high considering that: 1) it is our first attempt to fabricate a monolithically integrated analog and digital circuit; 2) the circuit is highly integrated, containing 6 microwave FET's, 5 diodes, 5 spiral inductors, 16 metal-insulator-metal capacitors, 26 resistors, and 35 digital logic gates. We attribute the high yield to the excellent uniformity and process simplicity inherent to refractory SAG FET fabrication.

TABLE 2

Integrated Buffer Amplifier/Prescaler Circuit Performance and Yield

(Circuit test with -22 dBm input signal power)

Parameter	193-2-1		193-2-2		193-2-4		193-2-6	
	MEAN	BEST	MEAN	BEST	MEAN	BEST	MEAN	BEST
Power Dissipation								
Prescaler (mW)	130	128	140	154	133	130	186	203
Buffer Amplifier (mW)	487	479	487	503	447	430	495	512
Total (mW) (incl. output drivers)	701	690	717	751	671	645	784	824
Frequency (GHz)	1.44	1.75	1.41	1.77	1.51	1.93	1.38	1.45
Yield	9/35 25%	---	16/35 45%	---	14/35 40%	---	2/35 6%	---

RF Yield of Buffer Amp = 45%

RF Yield of Prescaler = 84%

RF Yield of Combined Circuit = 30%

Finally, we have measured the RF performance of the separate limiting amplifier and prescaler chips as a function of temperature. (Our variable temperature bath could not accommodate the combined circuit test fixture.) This data is presented in Figs. 4 and 5. Figure 4 shows the performance of the limiting amplifier over the specified frequency range for temperatures from 25 to 150°C. As can be seen in the figure, several chips all display nearly constant gain response vs. frequency over the temperature range. Figure 5 shows the maximum frequency of the prescaler over the temperature range of 25 to 125°C. Again, the response vs. temperature is constant to within 10%.

In summary, we have demonstrated a process for fabricating fully planar, monolithically integrated analog and digital GaAs circuits. We present RF yield results and RF performance vs. temperature for a monolithically integrated ECL-compatible, L-band, limiting dual-modulus (÷ 10/11) prescaler. When tested with -22 dBm input signed power, one lot of six wafers had a total RF chip yield of 19%, with a best-wafer yield of 43%. The average operating frequency is 1.45 GHz (SD = 51 MHz) with an average power dissipation of 696 mW (SD = 23 mW).

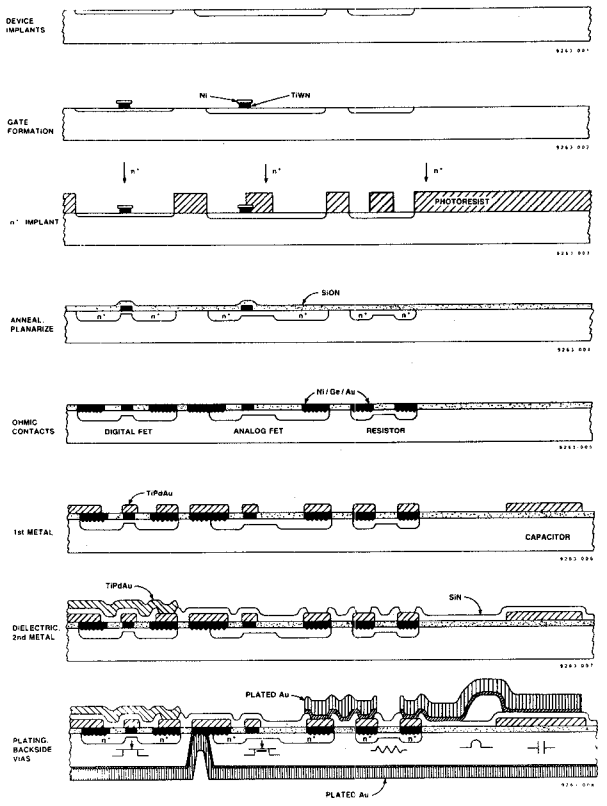

Fig. 1 Combined analog/digital refractory self-aligned gate process.

REFERENCES

(1) A.E. Geissberger, R.A. Sadler, E.L. Griffin, I.J. Bahl, and M.L. Balzan, "Refractory self-aligned gate technology for GaAs microwave FETs and MMICs," Electronics Lett., vol. 23, no. 20, pp. 1073-1075, 1987.

(2) H.P. Singh, R.A. Sadler, J.A. Irvine, and G.E. Gorder, "GaAs low-power parallel multipliers for a high-speed digital signal processor," 1987 IEEE GaAs IC Symposium Tech. Digest, pp. 253-256.

(3) A.E. Geissberger, R.A. Sadler, M.L. Balzan, and J.W. Crites, "TiW nitride thermally stable Schottky contacts to GaAs: characterization and application to SAG FET fabrication," J. Vac. Sci. Technol., vol. B5, no. 6, pp. 1701-1706, 1987.

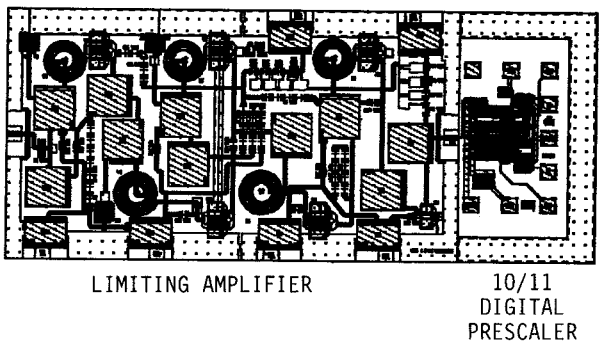

Fig. 2a Calma plot of the integrated limiting amplifier/prescaler circuit, the chip size is 1.7 x 3.7 mm^2.

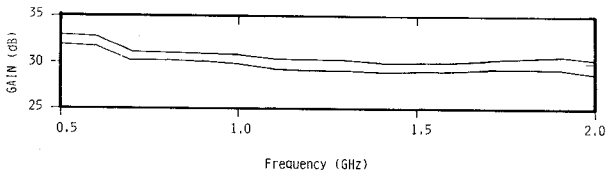

Fig. 2b Gain vs. frequency of the highest-gain and lowest-gain chips which passed the RF-gain criterion.

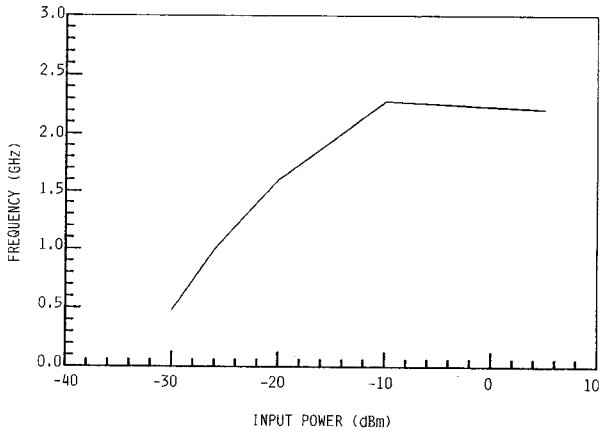

Fig. 3 Maximum output frequency of amplifier/prescaler vs. input power.

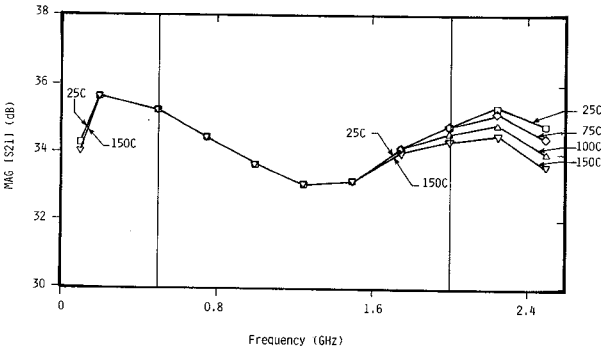

Fig. 4 Limiting amplifier chip gain (MAG of S21) vs. frequency for several temperatures (25°C to 150°C).

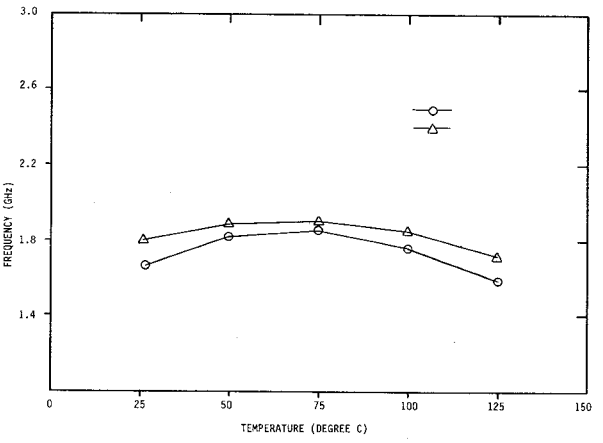

Fig. 5 Dual Modulus (÷ 10/11) Prescaler Maximum Operating Frequency vs. Temperature.